IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of: **MOTOOKA, et al.**

Group Art Unit: **2827**

Serial No.: **09/768,174**

Examiner: **J. Mitchell**

Filed: **January 24, 2001**

P.T.O. Confirmation No.: 1934

For: **SEMICONDUCTOR DEVICE HAVING A BALL GRID ARRAY AND FABRICATION PROCESS THEREOF**

RESPONSE UNDER 37 CFR §1.116
- EXPEDITED RESPONSE -
GROUP ART UNIT 2827

BOX AF

Commissioner for Patents
Washington, D.C. 20231

November 25, 2002

Sir:

In response to the Office Action dated **July 25, 2002**, extended to **November 25, 2002** by a **one (1)** month Petition for Extension of Time, please amend the above-identified application as follows:

IN THE CLAIMS:

Cancel claim 13.

Amend claim 11 as follows:

11. (Amended) A semiconductor device, comprising:

a semiconductor chip having a top surface, said semiconductor chip carrying a first electrode;

a circuit substrate attached to a top surface of said semiconductor chip, said circuit substrate carrying thereon a predetermined conductor pattern including a second electrode and a third electrode;

a solder resist layer provided on said circuit substrate;

a resin layer intervening between said top surface of said semiconductor chip and said circuit substrate;

a spherical electrode formed in an opening in said solder resist layer on said circuit substrate in correspondence to said third electrode;

a bonding wire electrically interconnecting said second electrode of said predetermined conductor pattern on said circuit substrate and said first electrode on said semiconductor chip; and

a resin potting encapsulating said bonding wire including said first and second electrodes,

said chip and said resin potting being defined by a common edge surface when viewed in a direction substantially perpendicular to a principal surface of said substrate,

wherein said resin layer has a composition substantially identical with a composition of said resin potting.

REMARKS

Claims 11-12 and 14-17 are pending in this application, of which claims 11 has been amended. Claim 13 has been cancelled. No new claims have been added.

Indicated allowance of claims 16 and 17 in the Office Action Summary on page 4, Section 10 of the Office Action is acknowledged. Further, Applicants agree to the comments of the Examiner about the allowability of claims 16 and 17 in Section 10 of the Office Action. Applicants therefore submit that the indicated rejection of claim 16 in page 2, Section 3 of the Office Action in view of **Heo et al.** (previously applied) is a typographical error.

Claims 11-13, 15 and 16 stand rejected under 35 U.S.C. §102(e) as anticipated by **Heo et al.** (previously applied).

Applicants respectfully traverse this rejection.

As noted in the previous Office Action of April 13, 2002, **Heo et al.** discloses a process for manufacturing a chip size semiconductor package with a light, thin and compact structure having a reduced size of its semiconductor chip while having an increased number of pins. For the package, it is possible to use either the semiconductor chip having bond pads arranged on end portions of the chip or the semiconductor chip having bond pads arranged on the central portion of the chip. In either case, input/output terminals of the package are arranged in the form of an area array.

Heo et al. fails to disclose that "said resin layer has a composition substantially identical with a composition of said resin potting", as recited in claim 13. By using the same resin for the

resin layer and the resin potting, the process of manufacturing the semiconductor device is substantially simplified. For example, it is possible to use the process of Figs. 11A-11F for forming the semiconductor device of claim 11.

Accordingly, claim 13 has been cancelled and its limitations added to claim 11.

Thus, the 35 USC §102(e) rejection of claims 11-12 and 15, as amended, should be withdrawn.

Claim 14 stands rejected under 35 U.S.C. §103(a) as unpatentable over **Heo et al.** in view of **Nakamura** (previously applied).

Applicants respectfully traverse this rejection.

As recited in Applicants' response of April 3, 2002, **Nakamura** discloses a tape automated bonding type semiconductor device having a glass epoxy substrate 7 but, like **Heo et al.**, fails to teach, mention or suggest the limitations recited in the amendments to claim 11, from which claim 14 depends.

Thus, the 35 USC §102(e) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 11-12 and 14-17, as amended, are in condition for allowance, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number

indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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